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Five-Level Full-bridge Inverters for Grid-tied Applications

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Abstract: In this paper, the detailed derivation process of two five-level full-bridge topology generation rules are presented and explained. One is the combination of a conventional three-level full-bridge inverter,a two-level capacitive voltage divider, and a neutral point clamped branch. The other method is to combine a three-level half-bridge inverter and a two-level half-bridge inverter. Furthermore, in order to enhance the reliability of existing five-level DBFBI topologies, an extended five-level DBFBI topology generation method is proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter; thus, a family of five-level DBFBI topologies connected with renewable energy system with high reliability is proposed. The operation modes, modulation methods, and control strategies of the series-switch five-level DBFBI topology are analyzed in detail. The power device losses of the three-level DBFBI topology and five-level DBFBI topologies, with different switching frequencies, are calculated and compared. Both the relationship between the neutral point potential self-balancing and the modulation index of inverters are revealed.

Keywords: Dual-Buck Inverter,Efficiency, Grid-Tied Inverter, Multilevel Inverter, Power Density.

I. INTRODUCTION

Electric utilities and end users of electric power are becoming increasingly concerned about meeting the growing energy demand. Seventy five percent of total global energy demand is supplied by the burning of fossil fuels. But increasing air pollution, global warming concerns, diminishing fossil fuels and their increasing cost have made it necessary to look towards renewable sources as a future energy solution. Since the past decade, there has been an enormous interest in many countries on renewable energy for power generation. The market liberalization and government's incentives have further accelerated the renewable energy sector growth. Renewable energy sources (RES) and distributed generations (DGs) have attracted special attention all over the world in order to reach the following two goals:

- the security of energy supply by reducing the dependence on imported fossil fuels;
- the reduction of the emission of greenhouse gases (e.g., CO2) from the burning of fossil fuels.

Other than their relatively low efficiency and high cost, the controllability of the electrical production is the main drawback of renewable energy generators, like wind turbines and photovoltaic panels, because of the uncontrollable meteorological conditions [1]. In consequence, their connection into the utility network can lead to grid instability or even failure if they are not properly controlled. Moreover, the standards for interconnecting these systems to the utility become more and more critical and require the DG systems to provide certain services, like frequency and voltage regulations of the local grid. Wind power is considered in this paper. Wind energy is the world's fastest growing energy source, expanding globally at a rate of 25%–35% annually over the last decade [2].The dual-buck inverter is an attractive solution to achieve high efficiency for low-power grid-connected applications. Many dual-buck inverter topologies have been developed in recent years [7]–[15], and some of them are utilized as gridtied inverters. Two filter inductors are required in single-phase dual-buck inverters, and both of the inductors are operating at each half cycle of the utility grid alternately, which increases the size and weight of the converter. Hence, the power density of conventional two-level and three-level dual-buck inverters needs to be improved.

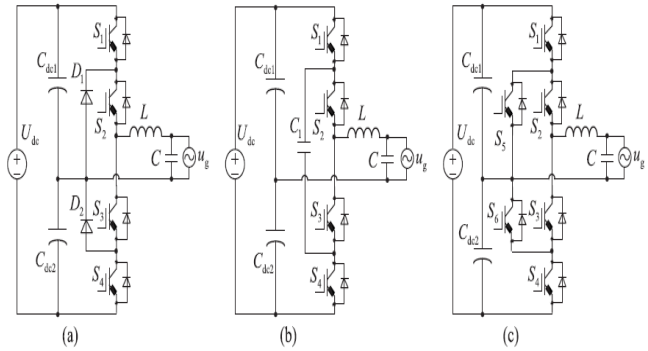


Fig1. Three popular topologies of H-bridge multilevel inverters. (a) DNPC. (b) FCC. (c) ANPC.

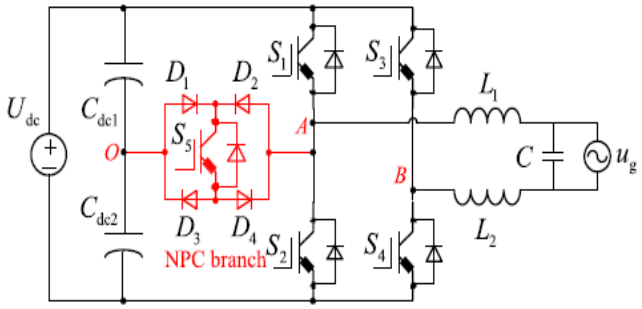


Fig2. Simplified five-level H-bridge inverter topology.

The multilevel technique is an effective way to achieve high power density. However, the number of power switches used in the multilevel inverter is more than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is much more complicated. Thus, the tradeoff between the performance and the hardware cost should be considered in the design of multilevel inverters [16]. There are three widely used topologies of single-phase multilevel inverters, as shown in Fig1, diode neutral point clamped (DNPC) multilevel inverters [17][18], flying capacitor clamped (FCC). multilevel inverters [19], [20], and active neutral point clamped (ANPC) multilevel inverters [21]. The basic concept of the above three multilevel topologies is to use smaller rating power devices to generate appreciable high-level output voltage waveforms. However, conventional multilevel inverters require a large number of power devices and auxiliary dc links when the output voltage levels are higher than three-level. A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the conventional full-bridge inverter [3], [24], as shown in Fig. 2. Compared with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly [2].

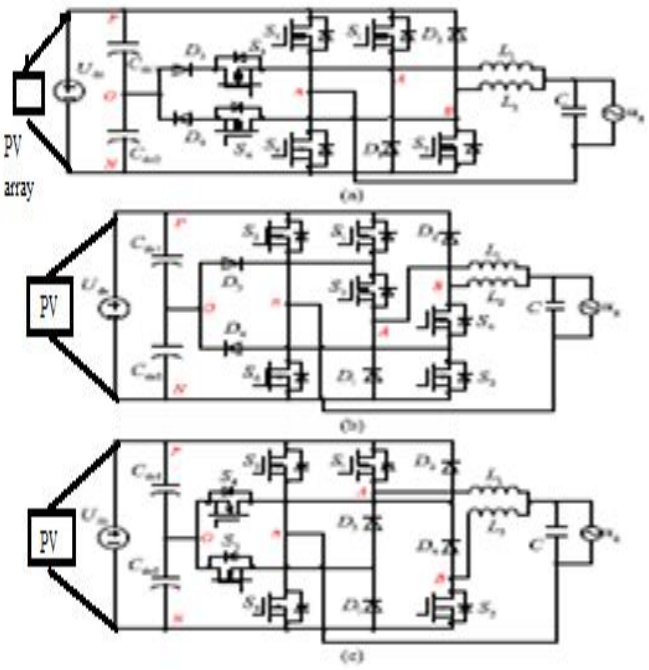


Fig3. Three topologies of five-level DBFBIs proposed, (a) NPC fivelevel DBFBI. (b) Series-switch five-level DBFBI. (c) Series-diode five-level DBFBI.

Therefore, for the low-voltage(less than 1000V) applications, this five-level H-bridge inverter topology is a better option than conventional multilevel inverter topologies. It is regarded as one of the best solutions for grid-tied inverters as well [16]. In [21], the issue of neutral point (NP) potential balancing was discussed as well, and the NP potential selfbalancing of two capacitors was considered to be automatically realized. However, the NP potential self-balancing of five-level full-bridge inverters is related to the modulation index. In this paper, the detailed derivation processes of two fivelevel full-bridge topology generation rules are presented and explained. An extended topology generation method is proposed for generating five-level DBFBI topologies, and a family of five-level DBFBI topologies with high reliability is derived. Furthermore, the relationship between the NP potential self balancing and the modulation index of inverters is revealed.

II. ANALYSIS ON THE SERIES-SWITCH FIVE-LEVEL DBFBI TOPOLOGY

A. Switching State Analysis

The series-switch five-level DBFBI topology is taken as an example for detailed analysis. The key waveforms of the seriesswitch five-level DBFBI are shown in Fig7. Two reference signals ur1 and ur2 are compared with a carrier signal ust to produce pulse width modulation signals for the switches. ugS1–ugS6 represent the gate drive signals of power switches S1 to S6 . In order to avoid the shoot-through problem, the dead time has been setwithin the drive signals of the switches S5 and S6.

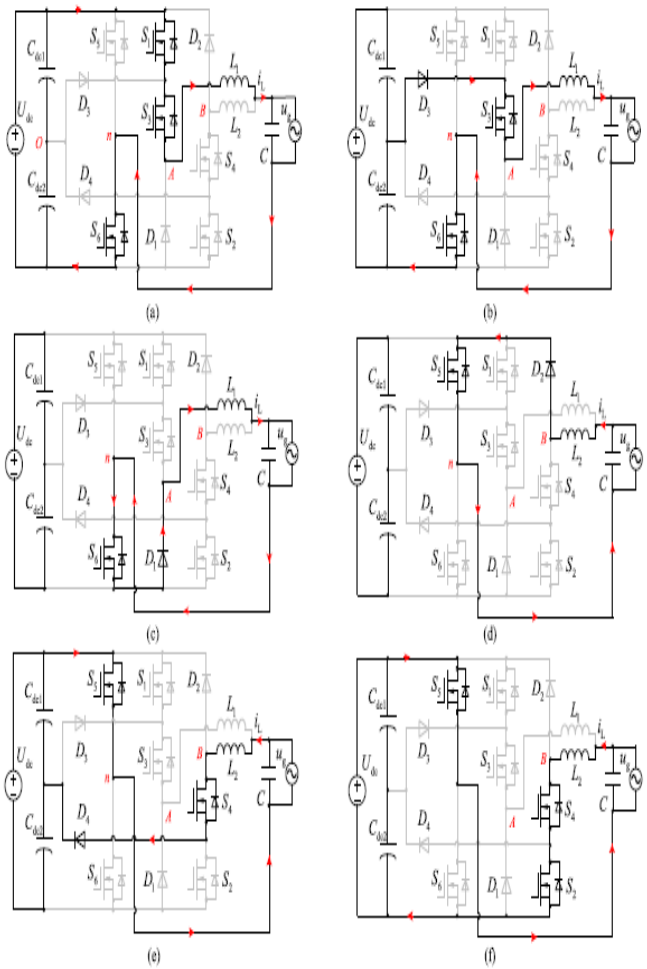


Fig4.Equivalent circuits of switching state,(a) State #1. (b) State #2. (c) State #3. (d) State #4. (e) State #5. (f) State #6.

uAn represents the voltage difference between the node A and node n, and uBn is the voltage difference between the node B and node n. Two filter inductors L1 and L2 are operating at each half cycle of the utility grid alternately. Therefore, uAB−n is defined as the output levels of the DBFBI topologies, and uAB−n is represented as

$$u_{\mathrm{AB-n}} = u_{\mathrm{An}} + u_{\mathrm{Bn}} - u_g. \tag{1}$$

On the other hand, the series-switch five-level DBFBI topology is operating with unity power factor. In order to avoid the inductor current distortion, at the beginning of the positive half cycle of the utility grid, the switches S1 , S3 , and S6 are turned ON at the same time. At the end of the positive half cycle, the switch S3 is turned OFF before the switch S6 , and the current of inductor L1 decreases to zero naturally. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S2 , S4 , and S5 are turned ON at the same time. At the end of the negative half cycle, the switch S4 is turned OFF before the switch S5 , and the current of inductor L2 decreases to zeronaturally. Since the series-switch five-level DBFBI topology is digitally controlled, this modulation method is easy to implement. Furthermore, it is also suitable for the NPC five-level DBFBI topology, the series-diode five-level DBFBI topology, and the family of five-level DBFBI topologies with high reliability. The series-switch five-level DBFBI has six operation modes, which are shown in Fig8.

1) State #1 [Refer to Fig. 8(a)]: Maximum positive output, uAn = Udc. There is no current flowing through the inductor L2 ; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = Udc. S1 , S3 , and S6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 8(a). The reverse blocking voltage on D3 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to Udc. The drain–source voltage on S5 is equal to Udc. During this state, the inductor current iL1 increases linearly

$$L_1 \frac{di_{L1}}{dt} = U_{\mathrm{dc}} - u_g. \tag{2}$$

2) State #2 [Refer to Fig. 8(b)]: Half-level positive output, uAn = 0.5Udc. There is no current flowing through the inductor L2 ; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = 0.5Udc. S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(b). The drain–source voltage on S1 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly when the voltage of the utility grid is higher than 0.5Udc

$$-L_1 \frac{di_{L1}}{dt} = \frac{U_{\mathrm{dc}}}{2} - u_g. \tag{3}$$

The inductor current iL1 increases linearly when the voltage of the utility grid is lower than $0.5U_{dc}$

$$L_1 \frac{di_{L1}}{dt} = \frac{U_{\mathrm{dc}}}{2} - u_g. \tag{4}$$

3) State #3 [Refer to Fig. 8(c)]: Zero output at the positive half period of the utility grid, uAn=0. There is no current flowing through the inductor L2; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = 0.S6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(c). Both the drain–source voltages on S1 and S3 are equal to 0.5Udc. During this state, the inductor current i_{L1} decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -u_g. \tag{5}$$

4) State #4 [Refer to Fig. 8(d)]: Zero output at the negative half period of the utility grid, uBn = 0. There is no current flowing through the inductor L1 ; thus, the voltage on the inductor L1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = 0.S5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(d). Both the drain–source voltages on S2 and S4 are equal to 0.5Udc. During this state, the inductor current iL2 increases linearly

$$L_2 \frac{di_{L2}}{dt} = -u_g. \tag{6}$$

5) State #5 [Refer to Fig. 8(e)]: Half-level negative output, uBn=−0.5Udc. There is no current flowing through the inductor L1; thus, the voltage on the inductorL1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = −0.5Udc. S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(e). The drain–source voltage on S2 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to 0.5Udc. During this state, the inductor current iL2 decreases linearly when the voltage of the utility grid is lower than 0.5Udc

$$-L_2 \frac{di_{L2}}{dt} = -\frac{U_{\mathrm{dc}}}{2} - u_g. \tag{7}$$

The inductor current iL2 increases linearly when the voltage of the utility grid is higher than 0.5Udc

$$L_2 \frac{di_{L2}}{dt} = -\frac{U_{\mathrm{dc}}}{2} - u_g. \tag{8}$$

6) State #6 [Refer to Fig. 8(f)]: Maximum negative output, uBn = −Udc. There is no current flowing through the inductor L1 ; thus, the voltage on the inductor L1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = −Udc. S2 , S4 , and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(f). The reverse blocking voltage on D4 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to Udc. During this state, the drain–source voltage on S6 is equal to Udc. In this mode, the inductor current iL2 decreases linearly

$$-L_2 \frac{di_{L2}}{dt} = -U_{\mathrm{dc}} - u_g. \tag{9}$$

Based on (2)–(9), it can be seen that the voltage jump of filter inductors is 0.5Udc, and the duty cycles of switches, S1–S4 , can be derived as

$$\begin{cases} d_{\mathrm{S1}} = (2u_g/U_{\mathrm{dc}}) - 1, & u_g > 0.5U_{\mathrm{dc}} \\ d_{\mathrm{S2}} = (-2u_g/U_{\mathrm{dc}}) - 1, & -u_g > 0.5U_{\mathrm{dc}} \\ d_{\mathrm{S3}} = 2u_g/U_{\mathrm{dc}}, & 0 < u_g < 0.5U_{\mathrm{dc}} \\ d_{\mathrm{S4}} = -2u_g/U_{\mathrm{dc}}, & -0.5U_{\mathrm{dc}} < u_g < 0. \end{cases} \tag{10}$$

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig2, the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage. Therefore, the switching loss of the presented fivelevel DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance.

B. Analysis of Voltage Stress

The maximum drain–source voltages on the switches S5 and S6 are equal to Udc. The maximum reverse blocking voltages on the diodes D1 and D2 are equal to Udc as well. The switch S1 is series connected with the switch S3 , and the switch S2 is series connected with the switch S4 . Therefore, the maximum drain–source voltages on the switches, S1, S2, S3, and S4, are equal to 0.5Udc. The maximum reverse blocking voltages on the diodes, D3 and D4, are equal to 0.5Udc as well. The analysis process on the maximum voltage stresses of the power devices in the other five-level DBFBI topologies is similar.

C. Analysis of NP Potential Balancing

From Fig. 8, both the switching state #2 and switching state #5 affect the NP potential of input split capacitors. During State #2, the voltage of C_{dc1} is increasing, and the voltage of C_{dc2} is decreasing. During State #5, the voltage of C_{dc1} is decreasing, and the voltage of C_{dc2} is increasing. At the positive half cycle of the utility grid, the voltage variation of C_{dc2} is represented as

$$\begin{cases} \Delta u_{C2-1} = \frac{-i_{C2}}{C_{dc2}}(1-d_{S1})T_s, & u_g > \frac{U_{dc}}{2} \\ \Delta u_{C2-2} = \frac{-i_{C2}}{C_{dc2}} d_{S3} T_s, & 0 < u_g < \frac{U_{dc}}{2} \end{cases} \quad (11)$$

where dS1 is the duty cycle of the switch S1 , and dS3 is the duty cycle of the switch S3.

From (3), (4), (7), and (8), iL1 is calculated by uCdc2 during the positive half cycle of the utility grid, and iL2 is calculated by uCdc1 during the negative half cycle of the utility grid.Assuming that uCdc1 is lower than uCdc2, the root-mean-square value of iL1 is larger than that of iL2. Therefore, the feedback of inductor current will have a positive dc component, and the output of the inductor current regulator has a negative dc component. The modulation signal has a negative dc component as well. Hence, both the dS1 and the dS3 become smaller at the positive half cycle of the utility grid. The sum ofΔuC2−1 andΔuC2−2 are obtained as (12) shown. where Ng represents the total switching times in a grid period, and Ng is defined as

$$\begin{cases} \sum_{t=Na+1}^{Ng/4} \Delta u_{C2-1} = \frac{-2T_s}{C_{dc2}} \sum_{t=Na+1}^{Ng/4} i_{C2}(t)(1-d_{S1}(t)), & u_g > \frac{U_{dc}}{2} \\ \sum_{1}^{Na} \Delta u_{C2-2} = \frac{-2T_s}{C_{dc2}} \sum_{1}^{Na} i_{C2}(t) d_{S3}(t), & 0 < u_g < \frac{U_{dc}}{2} \end{cases} \quad (12)$$

$$Ng = f_s / f_g \quad (13)$$

where fg represents the frequency of the utility grid, and fs represents the switching frequency.

Na represents the switching times in a quarter of grid period when 0 < ug < 0.5Udc, as shown in Fig9.

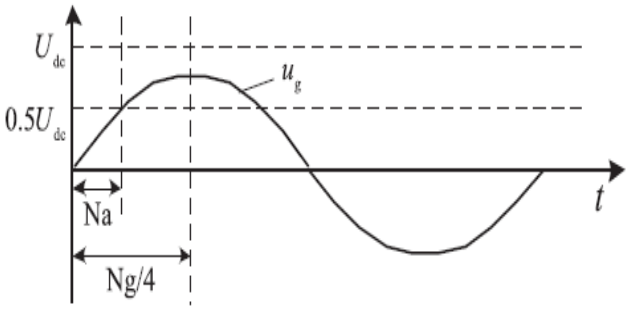


Fig5. Sketch diagram of the switching times.

Na is defined as

$$Na = a\sin\left(\frac{U_{dc}}{2U_{om}}\right) \cdot \frac{2}{\pi} \cdot Ng \quad (14)$$

where Uom is themaximum amplitude voltage of the utility grid. The modulation index of the five-level DBFBI topology can be calculated as

$$M = \frac{1}{2\sin\left(\frac{4Na}{Ng} \cdot \frac{\pi}{2}\right)}. \quad (15)$$

If the sum of ΔuC2−1 is higher than the sum of ΔuC2−2 , the decrease of uCdc2 becomes larger at the positive half cycle of the utility grid. Therefore, the NP potential balancing can be realized without any additional control. Contrarily, if the sum of ΔuC2−1 is smaller than the sum of ΔuC2−2 , the NP potential will be imbalanced.

Assume that the voltage of the utility grid is 230 V, and the frequency of the utility grid is 50 Hz. The grid-tied power is1 kW, and the switching frequency is 40 kHz. The NP potential balancing can be realized whenM> 0.56. From Fig. 6, it can be seen that when the modulation index is higher than 0.56, the divided input capacitor voltages are kept at self-balance. When the modulation index is lower than 0.56, the divided input capacitor voltages are imbalanced, and the voltages should be regulated by additional NP potential balancing mechanism, as shown in Fig. 6, where ud1 and ud2 represent the voltage of Cdc1 and Cdc2, respectively. iLr is the inductor current reference, and iLf is the feedback of the inductor current. ugff represents the feed-forward component of the utility grid voltage. Gcv is the NP potential balancing regulator, and Gci represents the inductor current regulator. The NP potential balancing is achieved by adding the output of NP potential balancing regulator and the inductor current reference.

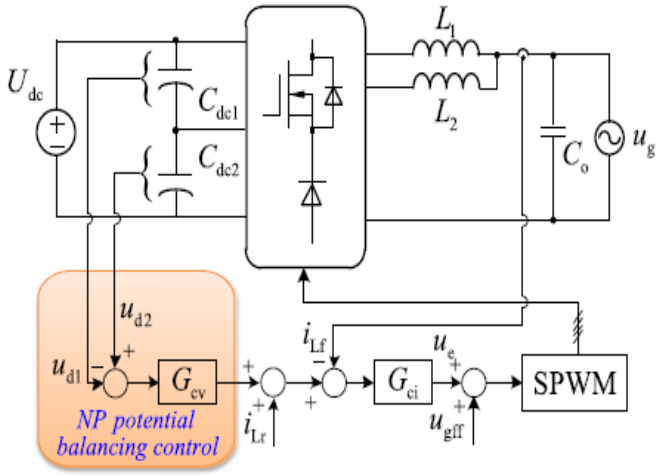


Fig. 6. Control block of five-level DBFBIs.

III. SIMULATION RESULTS

The circuit was built up to verify the feasibilities of the three-level DBFBI inverter the NPC five-level DBFBI(see Fig3), the series-switch five-level DBFBI [see Fig3(b)], the series-diode five-level DBFBI [seeFig3(c)], and the conventional five-level H-bridge inverter (see Fig. 2), and compare their performances. The specifications of these inverter topologies are listed in below Table . Since the lowest voltage rating of commercial SiC diodes is 600 V, only one kind of SiC diode was used in the five-level DBFBI topologies.

Parameter	Value
Input voltage	350–450 V
Grid voltage	230 V/50 Hz
Grid frequency	50 Hz
Rated power	1 kW
Switching frequency	40 kHz
Three-level filter inductor L_1 & L_2	4 mH
Five-level filter inductor L_1 & L_2	2 mH
Filter Capacitor C_o	0.47 μF

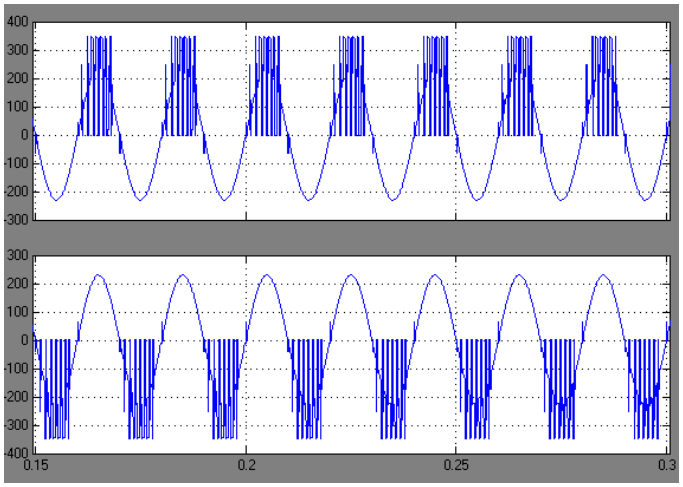


Fig7. Simulation waveforms of the SS five-level DBFBI. uAn and uBn.

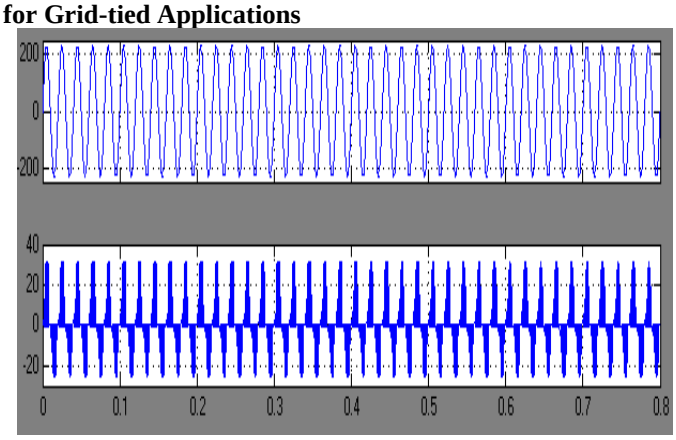


Fig8. Simulation waveforms of the SS five-level DBFBI, Vg and Ig.

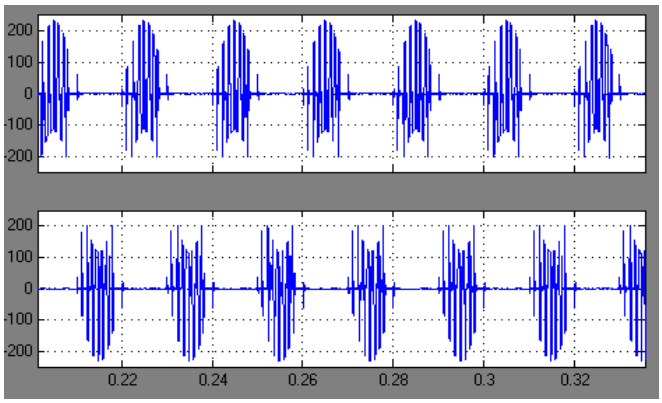
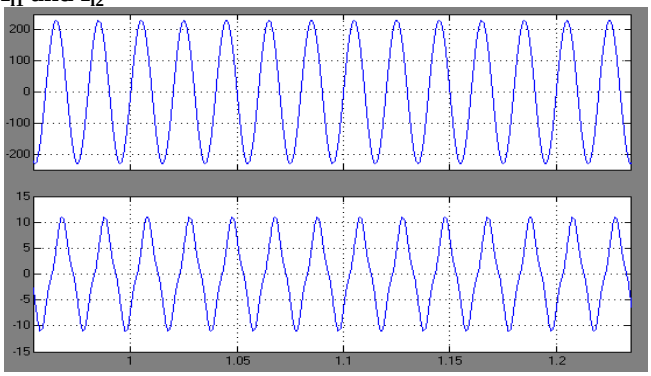


Fig.9. Simulation waveforms of the SS five-level DBFBI. I_{l1} and I_{l2}



.Fig10. Simulation waveforms of the SD five-level DBFBI. Vg and Ig.

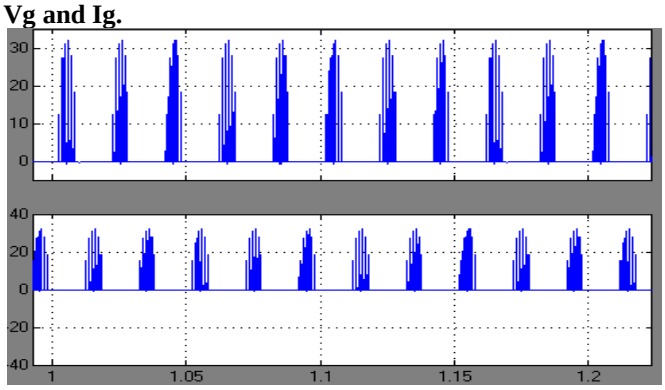


Fig11. Simulation waveforms of the SD five-level DBFBI. $V_{s1}$and V_{s2}

IV. CONCLUSION

In order to enhance the reliability of five-level DBFBI topologies, an extended five-level DBFBI topology generation method has been proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential selfbalancing and the modulation index of inverters is revealed. Simulation results have verified that the five-level DBFBI topologies have the following advantages:1) Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density. 2) The series-switch five-level DBFBI has the highest CEC efficiency compared with the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI, and the series-diode five-level DBFBI. Hence, the family of five-level DBFBI topologies is an attractive solution for grid-tied renewable generation systems with high efficiency and high power density.

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